Call for Papers

IEEE Transactions on Parallel and Distributed Systems
Special Issue - High-Performance Computing with Accelerators

There is a renewed interest in designing and building high-performance computer systems based on special-purpose chip architectures. Many research groups already have deployed experimental systems in which Field-Programmable Gate Arrays (FPGAs), Graphics Processing Units (GPUs), the Cell Broadband Engine, and ClearSpeed, to name a few, are used as co-processors, or application-specific accelerators to speed up the execution of computationally intensive codes, and the community is anxiously awaiting the introduction of Intel’s Larrabee and AMD’s Fusion chips. A few of these efforts have resulted in the deployment of large-scale systems, such as Los Alamos National Laboratory’s RoadRunner, which is based on IBM’s PowerXCell processor and is currently the fastest system in the world. High-performance computer designers are turning toward accelerators to increase performance, reduce power requirements, and enable previously unrealizable applications. To realize the potential of these new systems, however, much remains to be done on the software side as the scientific computing community is only beginning to understand the intricacies and interactions between the new hardware, execution models, software architectures, development processes, and the application transformations necessary to utilize the available resources effectively.

The IEEE Transactions on Parallel and Distributed Systems seeks articles for a July 2010 special issue focusing on efforts dedicated to the use of accelerators in high-performance computing. The guest editors invite papers that address the challenge of building and using such systems. Particular areas of interest include:

- design, analysis, and implementation of novel accelerator processors, systems, and architectures
- integration of accelerators with high-performance computing systems, performance measurement on experimental systems, reliability and fault-tolerance
- languages and compilers, profiling and debugging tools for accelerator-based computing
- run-time environments, operating system support, scheduling and task partitioning for accelerator-based computing
- programming models, analysis and design of algorithms for accelerator-based computing

Articles should discuss new research and include previously unpublished results. Papers previously published in conference proceedings should undergo substantial revision—at least 40% of the material should be new—and the authors should inform guest editors about the revisions made to the original publication.

Guest Editors

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Important Dates

Submissions due: September 24, 2009
Acceptance notification: March 16, 2010
Final manuscripts due: March 26, 2010
Publication date: August 2010

Submission Details

Authors should follow the standard IEEE TPDS manuscript preparation and submission instructions found at http://www.computer.org/tpds/. When submitting via Manuscript Central, specify that the manuscript is for the "High-Performance Computing with Accelerators” special issue. The submissions will be peer-reviewed and will be subject to editing for magazine style, clarity, organization, and space.